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What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A flash memory device comprising:

a semiconductor substrate;

a doped well within said semiconductor substrate;

a word line;

a bit line;

an array ground line;

a memory cell including a transistor having a drain coupled to said bit line, a control gate coupled to said word line, and a source coupled to said array ground line; and

a plurality of coupling transistors spaced within said doped well, said coupling transistors each having a first terminal coupled to said array ground line and a second terminal coupled to said doped well, said coupling transistors adapted to switchingly electrically couple said array ground line to said doped well.

2. A flash memory device as defined in claim 1 comprising:

a grounding transistor coupled between said array ground line and a source of ground potential.

3. A flash memory device as defined in claim 1 wherein said doped well is adapted to assume an electrical potential equal to one threshold voltage of said coupling transistors during a time interval when said coupling transistors are in a conductive state.

4. A flash memory device as defined in claim 1 wherein said doped well comprises:

a p-well, said coupling transistors are n-type transistors, and said array ground line includes a metallic trace.

5. A flash memory device as defined in claim 1 wherein said plurality of coupling transistors are responsive to a control signal having a first state adapted to make said coupling transistors non-conductive during a device erasing time interval and a second state adapted to make said coupling transistors conductive during a device reading time interval.

6. A grounding circuit for a flash memory cell comprising:

an array ground line coupled to a source terminal of a transistor of said flash memory cell; and

a plurality of array ground transistors having respective drains coupled to said array ground line, said plurality of array ground transistors having respective drains coupled to a doped well in which said flash memory cell is disposed, and said plurality of array ground transistors having respective array ground transistor gates adapted to receive a grounding signal in response to which said plurality of array ground transistors form a respective plurality of conductive paths between said array ground line and said doped well.

7. A grounding circuit for a flash memory cell as defined in claim 6 further comprising:

an array ground control line mutually coupling said array ground transistor gates for communicating said grounding signal to said array ground transistor gates.

8. A grounding circuit for a flash memory cell as defined in claim 7, wherein said plurality of array ground transistors are spaced apart from one another within said doped well.

9. A processor system comprising:

at least one processor;

at least one flash memory device coupled to exchange data with said processor, said flash memory device comprising:

a circuit for coupling an array ground line of said flash memory device to a doped well of said flash memory device during a time interval when data is being read from

a memory cell of said flash memory device, said circuit including a plurality of transistors coupled in parallel between said array ground line and said doped well.

10. A flash memory device comprising:

a plurality of flash memory transistors disposed within a doped well, each transistor of said plurality having a drain mutually coupled to a bit line and a respective source coupled to a respective array ground line;

a current sensing device including an analog to digital converter, said current sensing device having a first input coupled to a source of electric potential, a first output coupled to said bit line, and a second output port adapted to output a digital value corresponding to a current flowing through said first output;

a first switching device adapted to switchingly couple said array ground line to a source of substantially constant potential; and

a second switching device adapted to switchingly couple said array ground line to said doped well.

11. A flash memory device as defined in claim 10 comprising:

a third switching device adapted to switchingly couple said doped well to said source of substantially constant potential.

12. A flash memory device as defined in claim 10 wherein said source of substantially constant potential comprises:

a source of ground potential.

13. A flash memory device as defined in claim 10 wherein said doped well comprises:

a p-well and wherein said plurality of flash memory transistors includes a plurality of n-type flash memory transistors, each of said flash memory transistors including a respective control gate and a respective floating gate.

14. A flash memory device comprising:

a plurality of flash memory transistors each having a respective source, drain, and control gate, said respective source connected to one of a plurality of array ground lines, said plurality of flash memory transistors disposed within a doped well; and

means for switchingly coupling said plurality of array ground lines to said doped well during a read cycle of said flash memory device

15. A flash memory device as defined in claim 14, wherein said doped well is disposed within a substrate and wherein said memory device comprises:

means for switchingly coupling said plurality of array ground lines to a region of said substrate outside of said doped well.

16. A flash memory device as defined in claim 15, wherein:

said doped well includes a p-type semiconductor well and said substrate includes a p-type semiconductor substrate; and

wherein said memory device includes a region of n-type semiconductor material disposed between said doped well and said substrate.

17. A method of operating a flash memory device comprising:

switchingly electrically coupling an array ground line of said flash memory device containing a plurality of memory cells to a substrate portion of said flash memory device such that a first electrical potential of said substrate portion depends on a second electrical potential of said array ground line.

18. A method of manufacturing a flash memory device comprising:

forming a doped well in a semiconductor substrate;

disposing a plurality of flash memory transistors in said doped well, each of said flash memory transistors having a respective flash transistor source terminal;

disposing a plurality of field effect coupling transistors in said doped well, each of said field effect coupling transistors having a coupling transistor source and a

coupling transistor drain;

mutually coupling said flash transistor source terminals to an array ground node of said flash memory device;

mutually coupling said coupling transistor source terminals to said array ground node; and

switchingly coupling each one of said plurality of coupling transistor drains to said doped well, such that said plurality of coupling transistors are adapted to connect said array ground node to said doped well during a read cycle of said flash memory device.

19. A method of setting an electrical potential of a flash memory source of a flash memory transistor comprising:

coupling said flash memory source to an array ground node;

switchingly coupling said array ground node to a source of ground potential through an array ground transistor;

switchingly coupling said array ground node to a p-well disposed within a semiconductor substrate through a coupling transistor, said flash memory transistor disposed within said p-well; and

making said array ground transistor and said coupling transistor conductive during a read cycle time interval of said flash memory transistor.